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(54) Multibranch communications receiver

(57) A multipath wideband communications receiver (100) having a plurality of RF signal paths (116, 136) covering different but overlapping frequency bands and a plurality of baseband signal paths (140, 150, 160, 170, 180, 190), the paths being re-configurable for sharing of the first and second paths in different ways in order to facilitate processing of received signals in different modes.

Also, a rake receiver (800) employs a sigma-delta modulator arrangement (810) and programmable delays to provide fine delay adjustment. The sigma-delta modulator (810) may use sigma-delta circuitry from a sigma-delta A/D converters in a baseband paths of the receiver (100), that this may be achieved with no loss of functionality if in a particular reception configuration that sigma-delta A/D converter is not being utilized.

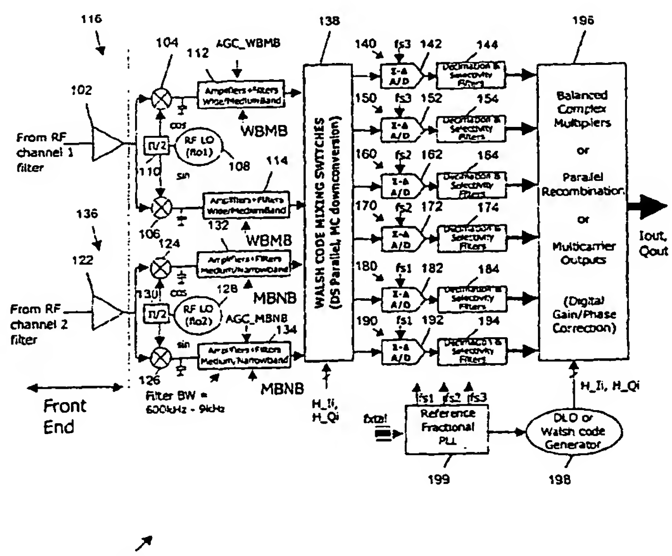

FIG. 1

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Description

Field of the Invention

[0001] This invention relates to communications receivers, and particularly to wireless communications receivers, such as mobile telephones.

Background of the Invention

[0002] In the field of this invention it is known that it is desirable for wireless communications receiver to be capable of multi-mode operation (i.e., to be capable of operating in any one of a plurality of different modes, including both narrow- and wide-band modes - for example, 2G/2.5G/3G cellular modes ('2G', '3G' and '2.5G' referring respectively to cellular systems of second generation, third generation and intermediate therebetween) and GPS (Global Positioning by Satellite) mode).

[0003] In order to produce a multi-mode wireless communications receiver it would be possible to combine in one circuit separate receiver sections, each receiver section being dedicated to a limited number of modes. For example, a GSM receiver section could be combined with a WB-CDMA (WideBand-Code Division Multiple Access) receiver section to make a 3G/2G receiver). This approach has the advantage that would allow simultaneous multi-mode operation, but it has the disadvantage that it would not be cost-effective (it would contain many redundant blocks) for a limited flexibility (the resolution of pipelined A/D (Analog/Digital) converters usually used in a WE-COMA receiver is difficult to extend beyond 10 bits) and would have a very high part count because the architectures of the individual receiver sections would be different (a superheterodyne receiver for one section, and a direct conversion receiver (DCR) for another section).

[0004] Although it would be possible to make a single receiver in which every circuit block is programmable, and such an approach would have the advantage of flexibility without redundancy, such an approach would have the disadvantage that it would not be able to support simultaneous multi-mode (which may be required in order to hand over seamlessly between two different modes).

[0005] A need therefore exists for a multipath communications receiver wherein the abovementioned disadvantage (s) may be alleviated.

Statement of Invention

[0006] In accordance with a first aspect of the present invention there is provided a multipath communications receiver as claimed in claim 1.

[0007] In accordance with a second aspect of the present invention there is provided a rake receiver for use in a communications receiver as claimed in claim 7.

Brief Description of the Drawings

[0008] One multipath wideband communications receiver incorporating the present invention will now be described, by way of example only, with reference to the accompanying drawings, in which:

FIG. 1 shows a block schematic circuit diagram of the multipath wideband communications receiver;

FIG. 2 shows a block schematic circuit diagram of the multipath wideband communications receiver of FIG. 1, configured for simultaneous reception and processing of signals in WBCDMA UMTS or CDMA2000 DS mode and GSM or EDGE mode;

FIG. 3 shows a block schematic circuit diagram of the multipath wideband communications receiver of FIG. 1, configured for reception and processing of signals in WBCDMA 2000 MC mode;

FIG. 4 shows a block schematic circuit diagram of the multipath wideband communications receiver of FIG. 1, configured for simultaneous reception and processing of EDGE signals received at different antennas to achieve diversity;

FIG. 5 shows a block schematic circuit diagram of the multipath wideband communications receiver of FIG. 1, configured for simultaneous reception and processing of signals in medium-band/narrow-band mode and Bluetooth mode;

FIG. 6 shows a block schematic circuit diagram of the multipath wideband communications receiver of FIG. 1, configured for simultaneous reception and processing of signals in wide-band mode and medium-band mode;

FIG. 7 shows a block schematic circuit diagram of the multipath wideband communications receiver of FIG. 1, configured for simultaneous reception and processing of signals in CDMA mode and medium/narrow-band mode; and

FIG. 8 shows a block schematic circuit diagram of a rake receiver which may advantageously be utilised in the multipath wideband communications receiver of FIG. 1.

Description of Preferred Embodiment(s)

[0009] Referring firstly to FIG. 1, a re-configurable multipath wideband communications receiver 100 has a first operational amplifier 102 for receiving an RF signal from a first RF channel filter (not shown). The output of the amplifier 102 is connected to mixers 104 and 106, whose other inputs are connected to receive opposite signals from a first RF local oscillator 108 via a phase splitter 110. The outputs of the mixers 104 and 106 (which, it will be appreciated, carry relative in-phase and quadrature-phase information from the received RF signal) are connected respectively to wide/medium-band amplifier/filter arrangements 112 and 114 (which will be discussed in greater detail below). It will thus be appreciated that the elements 102-114 represent an RF path 116.

[0010] A second operational amplifier 122 receives an RF signal from a second RF channel filter (not shown). The output of the amplifier 122 is connected to mixers 124 and 126, whose other inputs are connected to receive opposite signals from a second RF local oscillator 128 via a phase splitter 130. The outputs of the mixers 124 and 126 (which, it will be appreciated, carry relative in-phase and quadrature-phase information from the received RF signal) are connected respectively to a medium/narrowband amplifier/filter arrangements 132 and 134 (which will be discussed in greater detail below). It will thus be appreciated that the elements 122-134 represent an RF path 136.

[0011] The outputs of the amplifier/filter arrangements 112, 114, 132 and 134 are connected to inputs of a Walsh code switching matrix 138 which performs any necessary down-conversion and, depending on the modulation mode (s) of the received RF signals, applies outputs (derived from its inputs) to relevant ones (as will be described in greater detail below) of six parallel baseband paths 140, 150, 160, 170, 180 and 190. It will be understood that although in this example Walsh coding is used, other types of coding may alternatively be used if desired. The baseband paths 140, 150, 160, 170, 180 and 190 each comprise a sigma-delta analogue-to-digital converter (142, 152, 162, 112, 182 and 192 respectively) and a decimation/selectivity filter arrangement (144, 154, 164, 174, 184 and 194 respectively). The outputs of the parallel baseband paths 140, 150, 160, 170, 180 and 190 are connected to inputs of a mixing matrix 196. The switching matrix 138 and the mixing matrix 196 are controlled by inputs from a coding generator (such as, for example, a Walsh code generator) 198. A reference phase-locked-loop 199 provides low-frequency signals fs1, fs2, etc. for clocking the sigma-delta analogue-to-digital converters 142, 152, 162, 172, 182 and 192.

[0012] It will be understood that as an alternative, the elements of the switching matrix 138 could be directly embedded in the sigma-delta analogue-to-digital converters (142, 152, 162, 172, 182, 192) of the parallel baseband paths (140, 150, 160, 170, 180, 190).

[0013] As will be explained in greater detail below, the receiver 100 can function as a multipath wideband receiver, with:

- use of a mixture of DCR (direct conversion reception) and DVLIF (digital very low intermediate frequency) - both of which terms are intended to be covered herein by the term DCR - allowing an efficient architecture requiring a low number of external components;
- the two parallel RF paths (116 and 136) and the six parallel baseband paths (140, 150, 160, 170, 180 and 190) allowing optimal multipath processing depending on the modulation scheme(s) of the received signal(s) (as will be described in more detail below);
- the two parallel RF paths (116 and 136) being dedicated to different (but overlapping) frequency ranges allowing simultaneous multi-mode operation with optimized programming ranges;
- the six parallel baseband paths (140, 150, 160, 170, 180 and 190) allowing A/D conversion with sigma-delta converters providing high resolution with low clock frequency (providing low power consumption and requiring no additional PLL); and
- the six parallel baseband paths (140, 150, 160, 170, 180 and 190) allowing handling of multi-carrier wide-band signals (e.g., one path per carrier) or simultaneous multi-mode operation (e.g., 2 paths for wide-band and 1 path for medium/narrow-band).

[0014] The table below shows the main receiver characteristics associated with various modes which can be sup-

ported by the receiver of FIG. 1.

Standard	Mode	Bandwidth I or Q	Number of parallel ΣΔ A/D's	A/D Resolution	Sampling Frequency	Multi-mode (simultaneous: 2 Antennas)	Multi-mode (time-duplex)
WB-CDMA CDMA2000-DS	DCR	1.92 MHz	2	12 bits	30.72 MHz	with GSM and GPS	with all modes
CDMA2000-MC	DCR	3 x 625 KHz	1 per carrier	12 bits	19.648 MHz	no	with all modes
CDMA	DCR	625 KHz	1	12 bits	19.648 MHz	with GSM/EDGE, TDMA, iDEN, Bluetooth, GPS	with WB-CDMA
GSM/EDGE	DVLIF	180 KHz	1	13.5 bits	13 MHz	with CDMA, TDMA, iDEN, Bluetooth, GPS	with WB-CDMA
TDMA	DVLIF	30 KHz	1	14.5 bits	3.888 MHz	with CDMA, GSM/EDGE, iDEN, Bluetooth, GPS	with WB-CDMA
IDEN	DCR	9 KHz	1	15 bits	8.4 MHz	with CDMA, GSM/EDGE, TDMA, Bluetooth, GPS	with WB-CDMA
Bluetooth	DCR	600 KHz	1	9-10 bits	6-13 MHz	with CDMA, GSM/EDGE, TDMA, iDEN, GPS	with WB-CDMA
GPS	DCR	750 KHz	1	10 bits	24.552 MHz		with ALL MODES

[0015] Referring now to FIG. 2, in the configuration shown therein the receiver of FIG. 1 supports WBCDMA UMTS or CDMA2000 DS Mode with GSM or EDGE simultaneous reception.

[0016] The Wide/Medium-Band path is set to approx. 2MHz bandwidth. Two parallel sigma-delta converters are used for the WBCDMA DS mode. One-bit switch control signals (+1 or -1) are provided at the Sigma-Delta inputs. Operation is in DCR mode. The Medium/Narrow-Band path is set to approx. 500kHz bandwidth. One sigma-delta converter is used for GSM/EDGE operation. Operation is in Digital Very Low IF mode.

[0017] Referring now to FIG. 3, in the configuration shown therein the receiver of FIG. 1 supports WBCDMA CDMA2000 MC 3X Mode. The Wide/Medium-Band path is set to approx. 2MHz bandwidth. One-bit clock switch control signals (+1 or -1) are provided at the Sigma-Delta inputs. Complex down-conversion for multicarrier frequency is performed (fmc=1.22Mhz where H_cos is at carrier frequency with two levels (+1,-1) and H_sin is a pi/2 shift versus H_cos). The spur response is at 3*fmc where filtering is provided earlier in the flow. It is also possible to use a two-level modulation using Walsh code or similar sequences to reduce the level of spur response by switching the capacitors values of the sampling circuitry at fmc rate. Complex down-conversion uses I and Q. Each Sigma-Delta modulator is used to digitize a multicarrier channel on 12 bits at least.

[0018] Referring now to FIG. 4, in the configuration shown therein the receiver of FIG. 1 EDGE diversity reception, with both RF channels receiving EDGE signals received at different antennas.

[0019] Referring now to FIG. 5, in the configuration shown therein the receiver of FIG. 1 supports simultaneous Meidum/Narrow-Band Mode on one RF channel and Bluetooth mode on the other RF channel.

[0020] Referring now to FIG. 6, in the configuration shown therein the receiver of FIG. 1 supports simultaneous Medium-Band Mode on one RF channel and Narrow-Band mode on the other RF channel.

[0021] Referring now to FIG. 7, in the configuration shown therein the receiver of FIG. 1 supports simultaneous CDMA mode on one RF channel and Medium/Narrow-Band mode on the other RF channel.

[0022] Referring now to FIG. 8, a rake receiver 800 which may be advantageously used in the receiver of FIG. 1 is shown. The rake receiver 800 has a Sigma-Delta modulator 810 for receiving a signal to be rake filtered. The output of the Sigma-Delta modulator 810 is applied via a digital noise cancellation arrangement 820 to inputs of four parallel signals paths 830, 840, 850 and 860. All except one of the parallel signals paths 830, 840, 850 and 860 has its own respective programmable delay (842, 852, 862) and each of the paths includes a decimation filter, a first mixer, an accumulator filter and a second mixer. The outputs from each of the parallel signals paths 830, 840, 850 and 860 combined in a combiner 870 to produce the rake output.

[0023] It will be understood that, by utilizing the sigma-delta modulator arrangement 810 and programmable delays, the rake filter 800 can provide fine delay adjustment. It will further be appreciated that the sigma-delta modulator 810 may use the sigma-delta circuitry from one of the sigma-delta A/D converters (142, 152, 162, 172, 182 and 192) provided in the baseband paths of the receiver of FIG. 1, and that this may be achieved with no loss of functionality if in a particular reception configuration that sigma-delta A/D converter is not being utilized.

[0024] It will, of course, be appreciated that the present invention and the above-described embodiment(s) lend themselves readily to use in integrated circuit form, embodied in an arrangement of one or more integrated circuits, where many of the invention's advantages assume greater significance.

Claims

1. A multipath communications receiver (100), comprising:

   at least one first path (116) for processing received signals in a first frequency band;
   at least one second path (136) for processing received signals in a second frequency band which is different from but overlaps the first frequency band;
   the first and second paths employing direct conversion/low-IF processing means for processing received signals, and the first and second paths being re-configurable for sharing of the first and second paths in different ways in order to facilitate processing of received signals in different modes.

2. The multipath communications receiver of claim 1, wherein the first frequency band covers wide-band and medium-band frequencies and the second frequency band covers medium-band and narrow-band frequencies.

3. The multipath communications receiver of claim 1 or 2, further comprising a plurality of parallel baseband paths (140, 150, 160, 170, 180, 190) each employing sigma-delta analogue-to-digital conversion means (142, 152, 162, 172, 182, 192) arranged re-configurably to process in two shared said baseband paths a signal received in wide-band mode or to process simultaneously in two said baseband paths in parallel a first signal received in a first frequency band in a first mode and a second signal received in a second frequency band in a second mode.

4. The multipath communications receiver of claim 3, wherein the receiver comprises six said parallel baseband paths (140, 150, 160, 170, 180, 190).

5. The multipath communications receiver of claim 1, 2, 3 or 4 wherein the receiver is arranged to receive and process a received signal in at least one of the following modes: wide-band CDMA2000, CDMA2000, CDMA, UMTS, GSM/EDGE, TDMA, iDEN, Bluetooth, GPS.

6. An integrated circuit arrangement for use in a multipath communications receiver (100), the integrated circuit arrangement comprising:

   at least one first path (116) for processing received signals in a first frequency band;
   at least one second path (136) for processing received signals in a second frequency band which is different from but overlaps the first frequency band;
   the first and second paths employing direct conversion/low-IF processing means for processing received signals, and the first and second paths being re-configurable for sharing of the first and second paths in different ways in order to facilitate processing of received signals in different modes.

7. A rake receiver (800) for use in a communications receiver, the rake receiver comprising:

   sigma-delta modulator means (810) for receiving an input signal to be rake-filtered;
   a plurality of parallel delay paths (830, 840, 850, 860), comprising delay means (842, 852, 862) and filter means, for receiving the output of the sigma-delta modulator means and for producing respective delayed and filtered outputs; and
   combining means (870) for combining the outputs of the plurality of parallel delay paths.

8. The multipath communications receiver of claim 3, 4 or 5 further comprising the rake receiver of claim 7 wherein the sigma-delta modulator means (810) are arranged to be provided by re-configuration of the sigma-delta analogue-to-digital conversion means (142, 152, 162, 172, 182, 192) of at least one of said parallel baseband paths.

9. An integrated circuit arrangement for use in a rake receiver (800) for use in a communications receiver, the integrated circuit arrangement comprising:

   sigma-delta modulator means (810) for receiving an input signal to be rake-filtered;
   a plurality of parallel delay paths (840, 850, 860), each comprising delay means (842, 852, 862) and filter means, for receiving the output of the sigma-delta modulator means (810) and for producing respective delayed and filtered outputs; and
   combining means (870) for combining the outputs of the plurality of parallel delay paths.

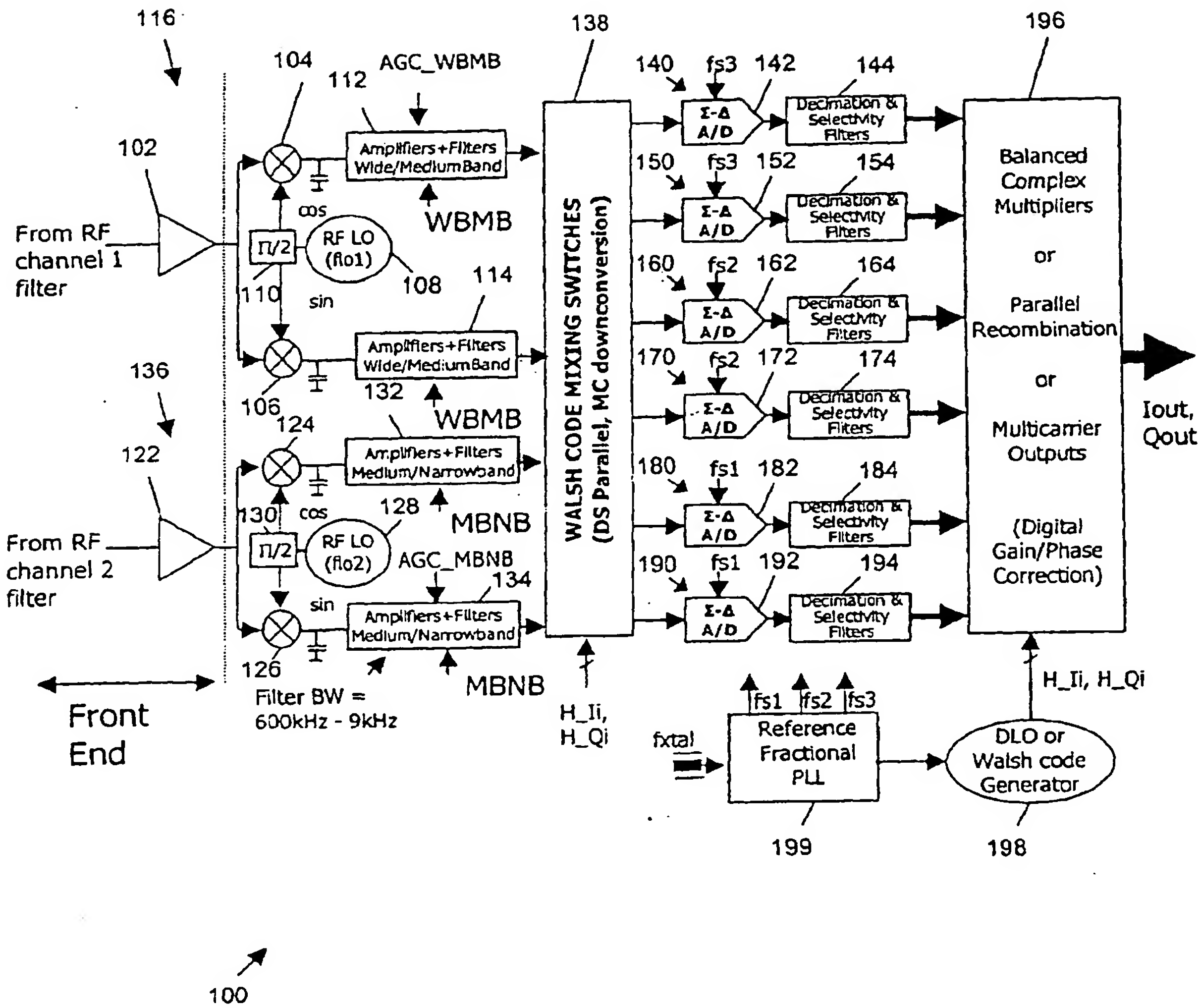

116
102
From RF channel 1 filter
104
AGC_WBMB
112
Amplifiers+Filters Wide/MediumBand
WBMB
cos
Π/2
RF LO (flo1)
108
110
sin
114
Amplifiers+Filters Wide/MediumBand
136
106
132
WBMB
124
122
Amplifiers+Filters Medium/Narrowband
130
cos
128
MBNB
From RF channel 2 filter
Π/2
RF LO (flo2)
AGC_MBNB
134
sin
Amplifiers+Filters Medium/Narrowband
126
Filter BW = 600kHz - 9kHz
MBNB
Front End
138
WALSH CODE MIXING SWITCHES (DS Parallel, MC downconversion)
H_Ii, H_Qi
140
fs3
142
144
Σ-Δ A/D
Decimation & Selectivity Filters
150
fs3
152
154
160
fs2
162
164
170
fs2
172
174
180
fs1
182
184
190
fs1
192
194
196
Balanced Complex Multipliers
or
Parallel Recombination
or
Multicarrier Outputs
(Digital Gain/Phase Correction)
Iout, Qout
H_Ii, H_Qi
fs1
fs2
fs3
fxtal
Reference Fractional PLL
DLO or Walsh code Generator
199
198
100

FIG. 1

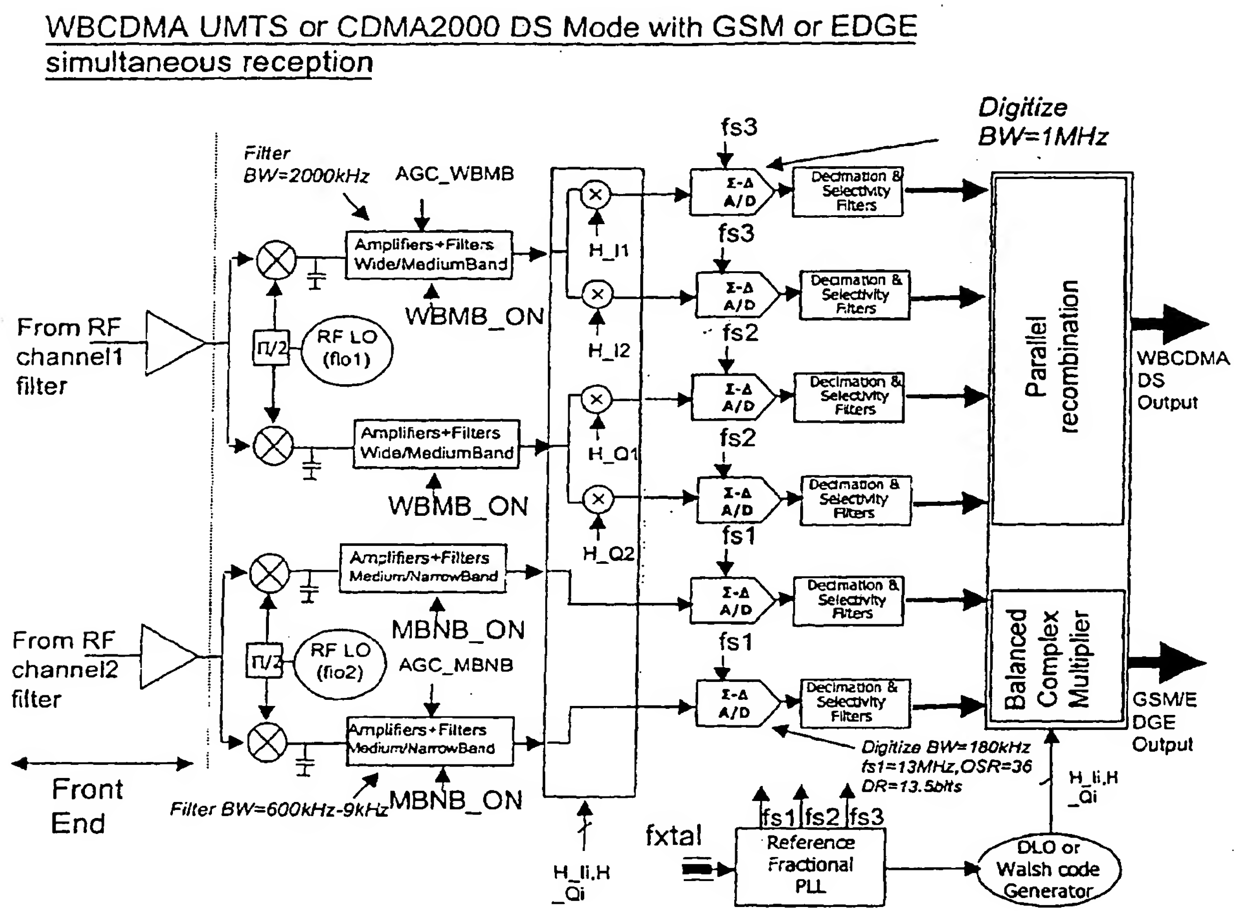

WBCDMA UMTS or CDMA2000 DS Mode with GSM or EDGE simultaneous reception
Digitize BW=1MHz
Filter BW=2000kHz
AGC_WBMB
fs3
Amplifiers+Filters Wide/MediumBand
WBMB_ON
From RF channel1 filter
RF LO (flo1)
Π/2
H_I1
H_I2
fs2
H_Q1
H_Q2
fs1
Decimation & Selectivity Filters
Σ-Δ A/D
Parallel recombination
WBCDMA DS Output
Amplifiers+Filters Medium/NarrowBand
MBNB_ON
From RF channel2 filter
RF LO (flo2)
AGC_MBNB
Balanced Complex Multiplier
GSM/EDGE Output
Digitize BW=180kHz fs1=13MHz,OSR=36 DR=13.5bits
H_Ii,H_Qi
Front End
Filter BW=600kHz-9kHz
fxtal
Reference Fractional PLL
DLO or Walsh code Generator

FIG. 2

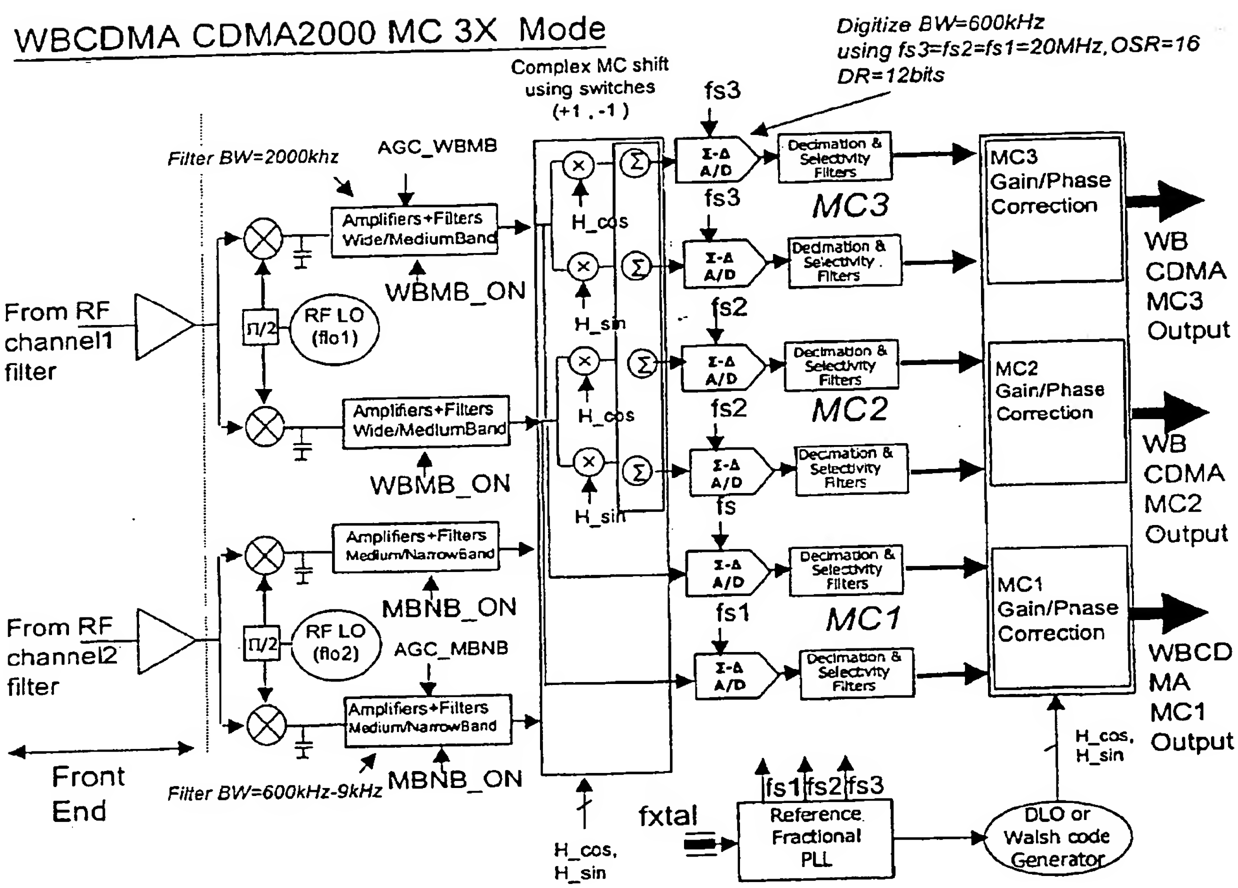

WBCDMA CDMA2000 MC 3X Mode
Complex MC shift using switches (+1 , -1)
Digitize BW=600kHz using fs3=fs2=fs1=20MHz, OSR=16 DR=12bits
Filter BW=2000khz
AGC_WBMB
Amplifiers+Filters Wide/MediumBand
WBMB_ON
From RF channel1 filter
π/2
RF LO (flo1)
Amplifiers+Filters Wide/MediumBand
WBMB_ON
Amplifiers+Filters Medium/NarrowBand
MBNB_ON
From RF channel2 filter
π/2
RF LO (flo2)
AGC_MBNB
Amplifiers+Filters Medium/NarrowBand
MBNB_ON
Front End
Filter BW=600kHz-9kHz
H_cos
H_sin
H_cos
H_sin
H_cos, H_sin
fs3
fs3
fs2
fs2
fs
fs1
Σ-Δ A/D
Decimation & Selectivity Filters
MC3
MC2
MC1
MC3 Gain/Phase Correction
MC2 Gain/Phase Correction
MC1 Gain/Phase Correction
WB CDMA MC3 Output
WB CDMA MC2 Output
WBCDMA MC1 Output
H_cos, H_sin
fs1 fs2 fs3
fxtal
Reference Fractional PLL
DLO or Walsh code Generator

FIG. 3

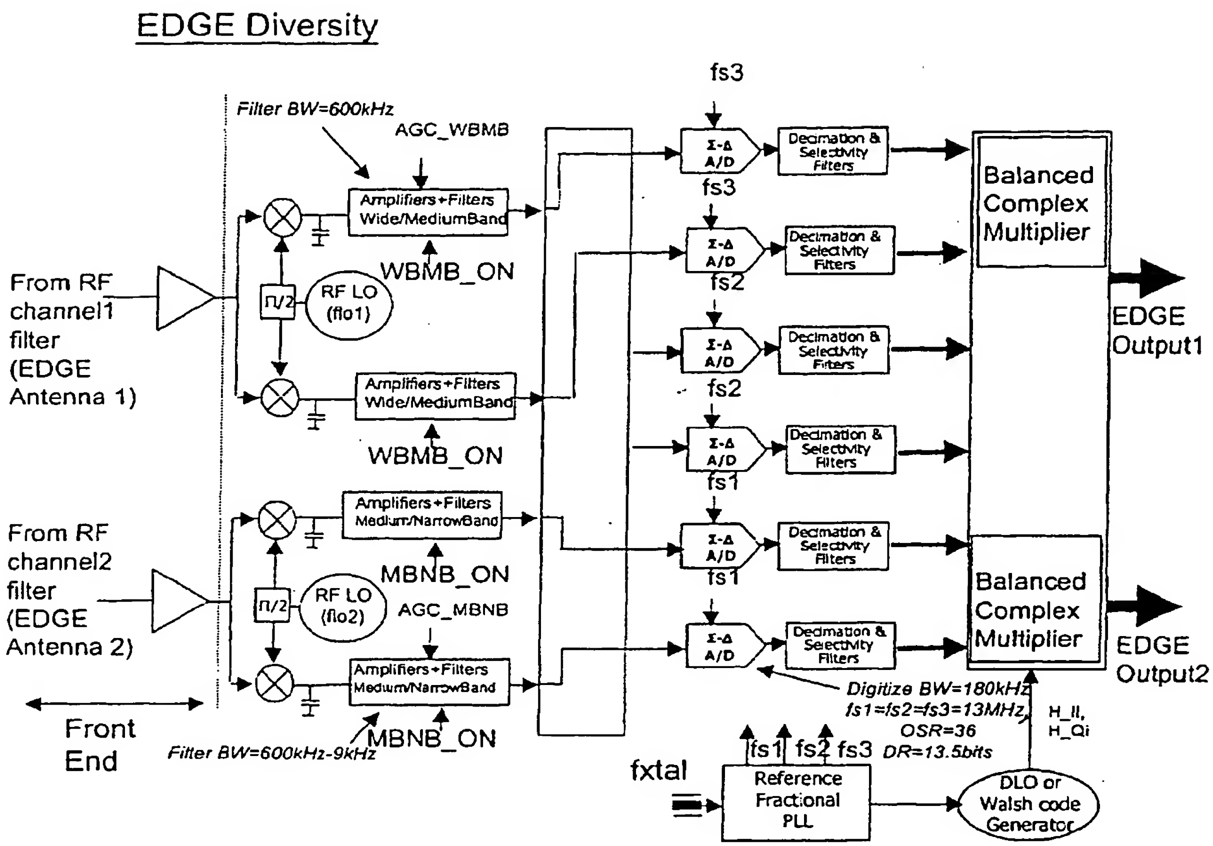

EDGE Diversity
fs3
Filter BW=600kHz
AGC_WBMB
Amplifiers+Filters Wide/MediumBand
Σ-Δ A/D
Decimation & Selectivity Filters
Balanced Complex Multiplier
WBMB_ON
From RF channel1 filter (EDGE Antenna 1)
Π/2
RF LO (flo1)
fs2
EDGE Output1
fs1
From RF channel2 filter (EDGE Antenna 2)
Amplifiers+Filters Medium/NarrowBand
MBNB_ON
RF LO (flo2)
AGC_MBNB
EDGE Output2
Digitize BW=180kHz
fs1=fs2=fs3=13MHz
OSR=36
DR=13.5bits
H_II,
H_Qi
Front End
Filter BW=600kHz-9kHz
fxtal
Reference Fractional PLL
DLO or Walsh code Generator

FIG. 4

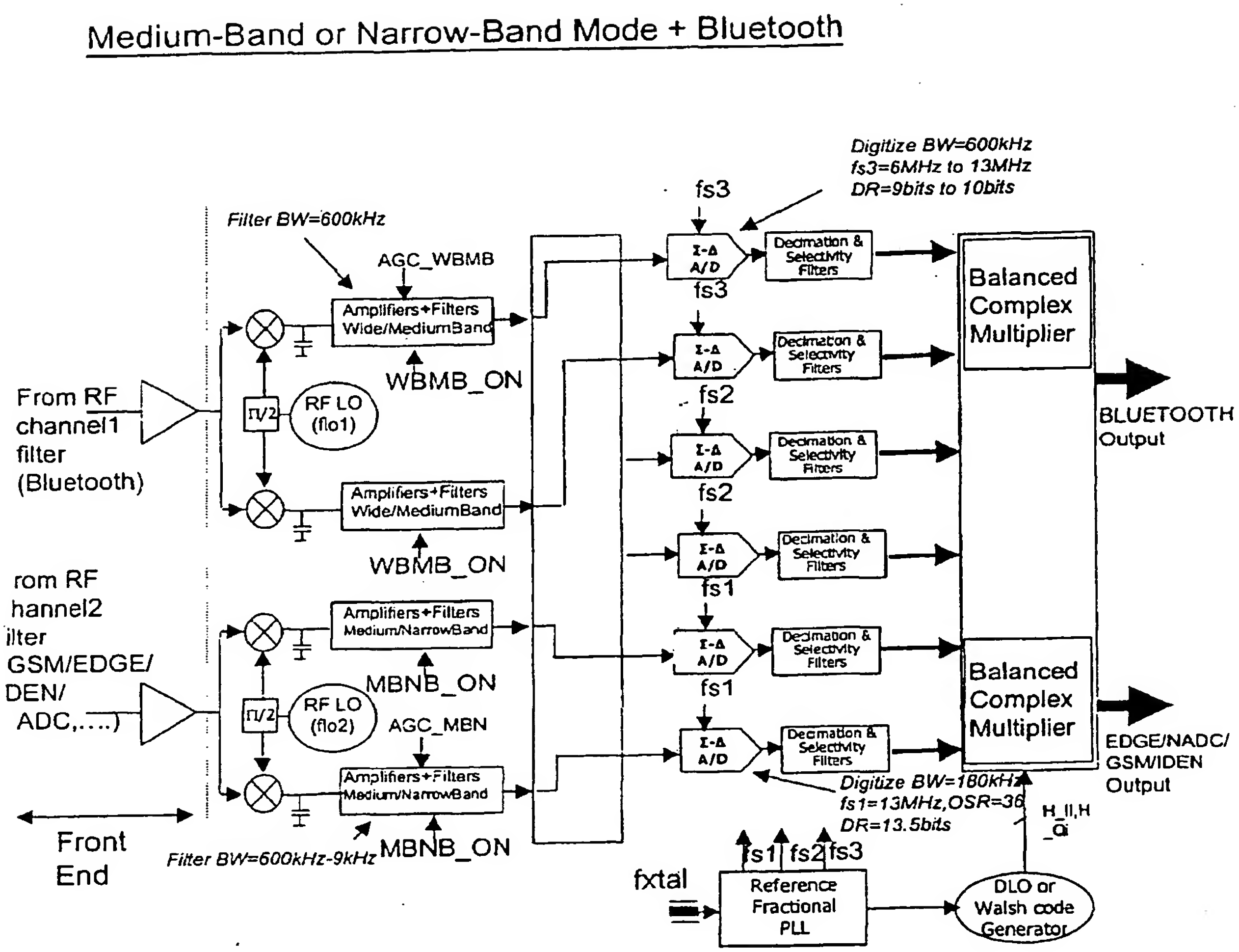

Medium-Band or Narrow-Band Mode + Bluetooth
Digitize BW=600kHz
fs3=6MHz to 13MHz
DR=9bits to 10bits
fs3
Filter BW=600kHz
AGC_WBMB
Amplifiers+Filters Wide/MediumBand
WBMB_ON
From RF channel1 filter (Bluetooth)
RF LO (flo1)
Amplifiers+Filters Wide/MediumBand
WBMB_ON
rom RF hannel2 ilter GSM/EDGE/ DEN/ ADC,....)
Amplifiers+Filters Medium/NarrowBand
MBNB_ON
RF LO (flo2)
AGC_MBN
Amplifiers+Filters Medium/NarrowBand
Front End
Filter BW=600kHz-9kHz
MBNB_ON
Σ-Δ A/D
Decimation & Selectivity Filters
fs2
fs1
Balanced Complex Multiplier
BLUETOOTH Output
Balanced Complex Multiplier
EDGE/NADC/ GSM/IDEN Output
Digitize BW=180kHz
fs1=13MHz,OSR=36
DR=13.5bits
fs1 fs2 fs3
fxtal
Reference Fractional PLL
DLO or Walsh code Generator

FIG. 5

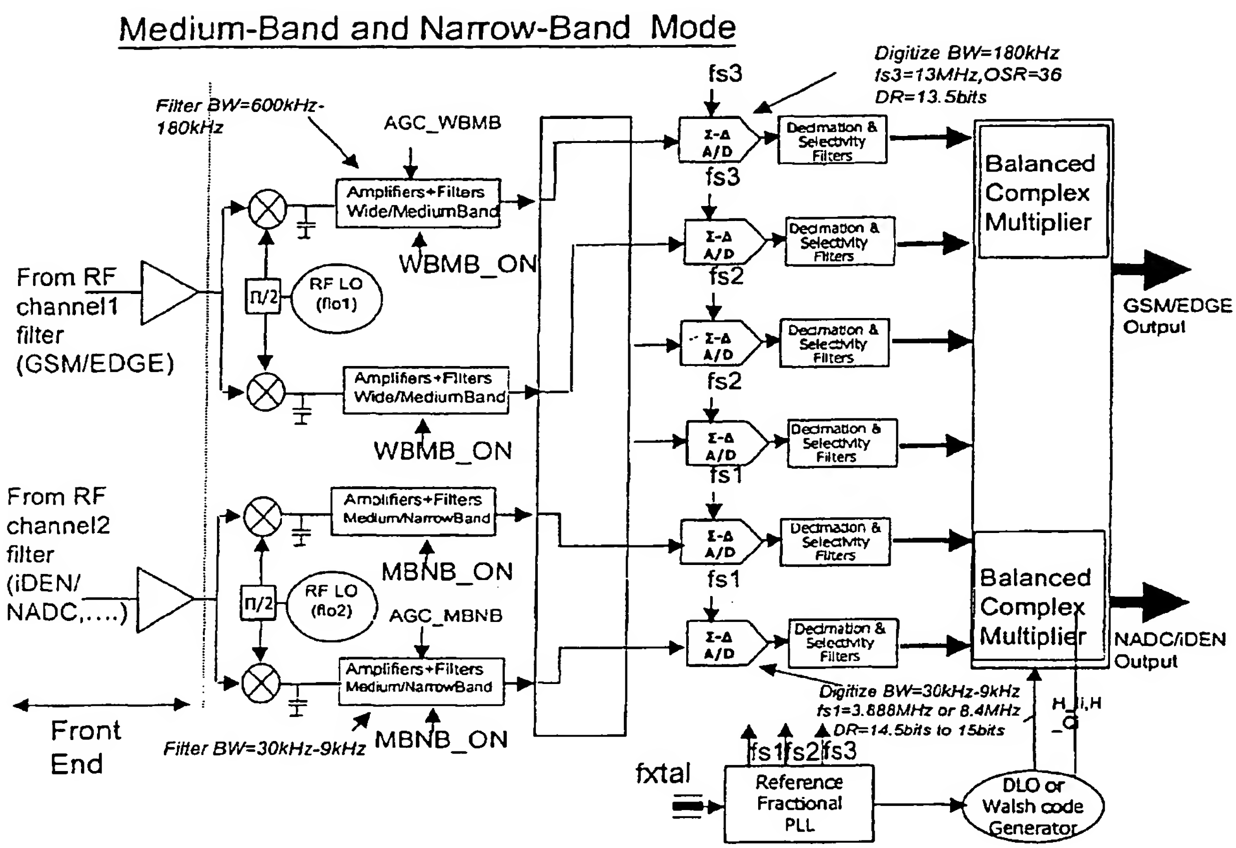

Medium-Band and Narrow-Band Mode
Filter BW=600kHz-180kHz
AGC_WBMB
Amplifiers+Filters Wide/MediumBand
WBMB_ON
From RF channel1 filter (GSM/EDGE)
RF LO (flo1)
π/2
Amplifiers+Filters Wide/MediumBand
WBMB_ON
From RF channel2 filter (iDEN/ NADC,....)
Amplifiers+Filters Medium/NarrowBand
MBNB_ON
RF LO (flo2)
AGC_MBNB
Amplifiers+Filters Medium/NarrowBand
Front End
Filter BW=30kHz-9kHz
MBNB_ON
fs3
Digitize BW=180kHz
fs3=13MHz,OSR=36
DR=13.5bits
Σ-Δ A/D
Decimation & Selectivity Filters
fs2
fs1
Balanced Complex Multiplier
GSM/EDGE Output
NADC/iDEN Output
Digitize BW=30kHz-9kHz
fs1=3.888MHz or 8.4MHz
DR=14.5bits to 15bits
H_I,H_Q
fs1 fs2 fs3
fxtal
Reference Fractional PLL
DLO or Walsh code Generator

FIG. 6

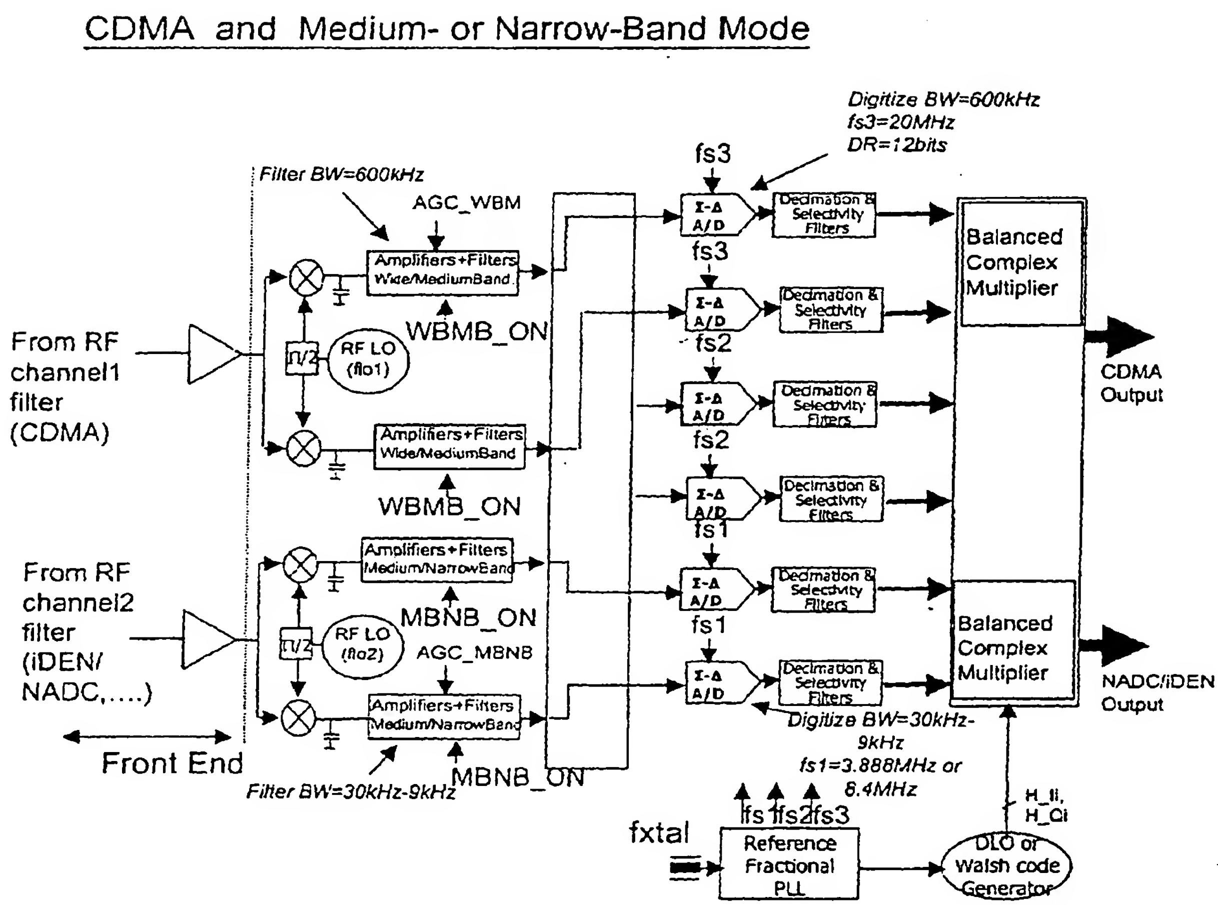
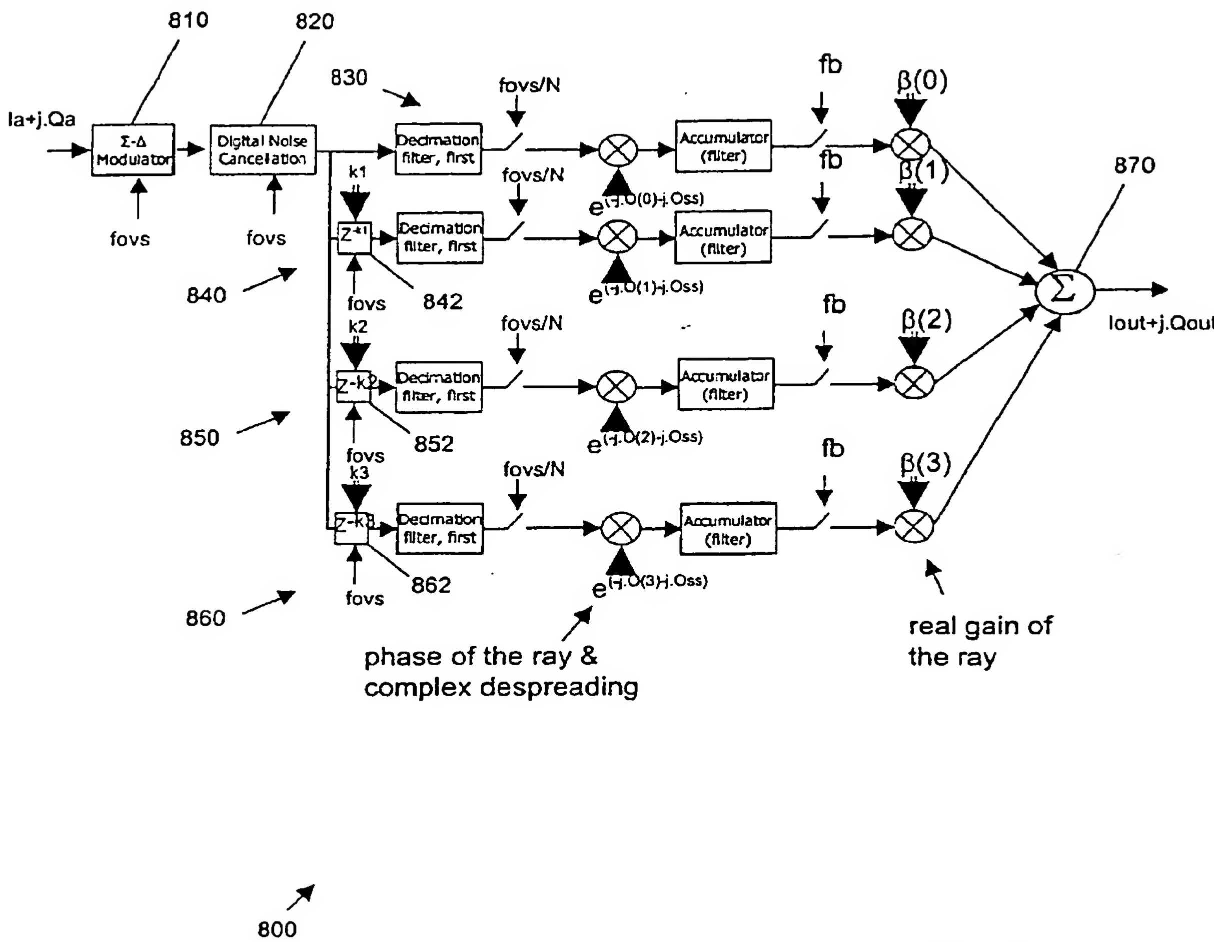

CDMA and Medium- or Narrow-Band Mode
Digitize BW=600kHz
fs3=20MHz
DR=12bits
fs3
Filter BW=600kHz
AGC_WBM
Amplifiers+Filters
Wide/MediumBand
WBMB_ON
From RF channel1 filter (CDMA)
RF LO (flo1)
WBMB_ON
From RF channel2 filter (iDEN/ NADC,....)
RF LO (flo2)
MBNB_ON
AGC_MBNB
Amplifiers+Filters
Medium/NarrowBand
Front End
Filter BW=30kHz-9kHz
MBNB_ON
Σ-Δ A/D
Decimation & Selectivity Filters
fs2
fs1
Balanced Complex Multiplier
CDMA Output
NADC/iDEN Output
Digitize BW=30kHz-9kHz
fs1=3.888MHz or 8.4MHz
fs1 fs2 fs3
fxtal
Reference Fractional PLL
H_Ii, H_Qi
DLO or Walsh code Generator

FIG. 7



810
820
830
Ia+j.Qa
Σ-Δ Modulator
Digital Noise Cancelation
fovs
fovs
Decimation filter, first
fovs/N
Accumulator (filter)
fb
β(0)
β(1)
870
k1
Decimation filter, first
fovs/N
Accumulator (filter)
fb
840
fovs
842
Σ
Iout+j.Qout
k2
fovs/N
fb
β(2)
Decimation filter, first
Accumulator (filter)
850
852
fovs
k3
fovs/N
fb
β(3)
Decimation filter, first
Accumulator (filter)
860
fovs
862
phase of the ray & complex despreading
real gain of the ray
800

FIG. 8

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 00 40 3443

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
Y	WO 00 52840 A (CONEXANT SYSTEMS INC) 8 September 2000 (2000-09-08) * abstract * * page 13, line 1 - page 23, line 17 * * page 41, line 11 - page 49, line 17 * * figure 8 *	1-6	H04B1/40 H04B1/30 H04B1/707
Y A	US 5 999 990 A (CAMPINI EDOARDO ET AL) 7 December 1999 (1999-12-07) * abstract * * column 2, line 6 - column 3, line 12 * * column 4, line 41 - column 5, line 17 * * figure 1 *	1,3-6 2	
Y A	WO 00 41322 A (SCHMIDT PETER ;DOETSCH MARKUS (DE); JUNG PETER (DE); INFINEON TECH) 13 July 2000 (2000-07-13) * abstract * * page 2, line 8 - page 13, line 6 * * figure 1 *	1,2,6 3-5	
Y	EP 0 756 391 A (MATRA COMMUNICATION) 29 January 1997 (1997-01-29) * abstract * * page 1, line 57 - page 4, line 43 * * figure 1 *	7-9	TECHNICAL FIELDS SEARCHED (Int.Cl.7) H04B
Y	WO 99 65154 A (ERICSSON TELEFON AB L M) 16 December 1999 (1999-12-16) * abstract * * page 4, line 19 - page 8, line 13 * * page 13, line 19 - page 18, line 9 * * figure 2 * * figure 5 * -/--	7-9	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	15 October 2001	Lindhardt, U

CATEGORY OF CITED DOCUMENTS

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EUROPEAN SEARCH REPORT

Application Number
EP 00 40 3443

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
A	M. NEITOLA T. RAHKONEN: "AN ANALOG CORRELATOR FOR A WCDMA RECEIVER" IEEE INTERNATIONAL SYMPOSIUM ON CIRCUITS AND SYSTEMS, no. IV, 28 - 31 May 2000, pages 753-756, XP002180132 Geneva, Switzerland * the whole document *	7-9	
			TECHNICAL FIELDS SEARCHED (Int.Cl.7)

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	15 October 2001	Lindhardt, U

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X : particularly relevant if taken alone
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EPO FORM 1503 03.82 (P04C01)

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This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report.
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15-10-2001

Patent document cited in search report		Publication date	Patent family member(s)		Publication date
WO 0052840	A	08-09-2000	WO	0052840 A1	08-09-2000
US 5999990	A	07-12-1999	AU	4191399 A	06-12-1999
			EP	1080541 A1	07-03-2001
			WO	9960715 A1	25-11-1999
WO 0041322	A	13-07-2000	WO	0041322 A1	13-07-2000
			EP	1142144 A1	10-10-2001
EP 0756391	A	29-01-1997	FR	2737362 A1	31-01-1997
			CA	2181670 A1	26-01-1997
			EP	0756391 A1	29-01-1997
			US	5818866 A	06-10-1998
WO 9965154	A	16-12-1999	AU	4811699 A	30-12-1999
			CN	1312978 T	12-09-2001
			EP	1086535 A1	28-03-2001
			WO	9965154 A1	16-12-1999

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82